ABSTRACT

A method for calibrating a low pass filter is disclosed. The low pass filter comprises a plurality of transconductor cells. The method comprises generating a test signal to the low pass filter and suppressing even-order harmonics due to transistor mismatches within the plurality of transconductor cells. By adding a small number of transistors, the mismatch-induced even order harmonics can be greatly reduced. Even-order harmonics are minimized through the application of a control voltage. A method for calibrating against transistor mismatch utilizing a CMOS transconductor that is based on the regulated cascode topology is disclosed. The method is designed to provide suppression of the even-order harmonics, a very small increase in power and a silicon area of the transconductor cell. A well-defined offset is provided by biasing one of the mismatched transistors.